# Exhibit 8

# Micron® DDR5: Key Module Features

## DDR4 vs. DDR5 DIMM

This technical brief is a follow-up to Micron's earlier DDR5 white paper titled, "Micron DDR5 SDRAM: New Features," which highlighted key fifth-generation double data rate (DDR5) SDRAM features and functionality that deliver significant performance improvements over DDR4. In this paper, we provide further detail about key aspects of the DDR5 dual in-line memory module (DIMM) and advantages over DDR4. With the changing landscape of ever-increasing core counts, DDR5 was designed to increase bandwidth delivered to systems. The module design has also changed to support this capability.

### Module Layout and Data Access

A key difference of the DDR5 module as compared to a DDR4 module is the presence of subchannels (Figure 1). A standard DDR5 module has two independent subchannels. Each subchannel has up to two physical package ranks. Each DRAM package can be configured in a primary/secondary topology to enable additional logical ranks for increased density.

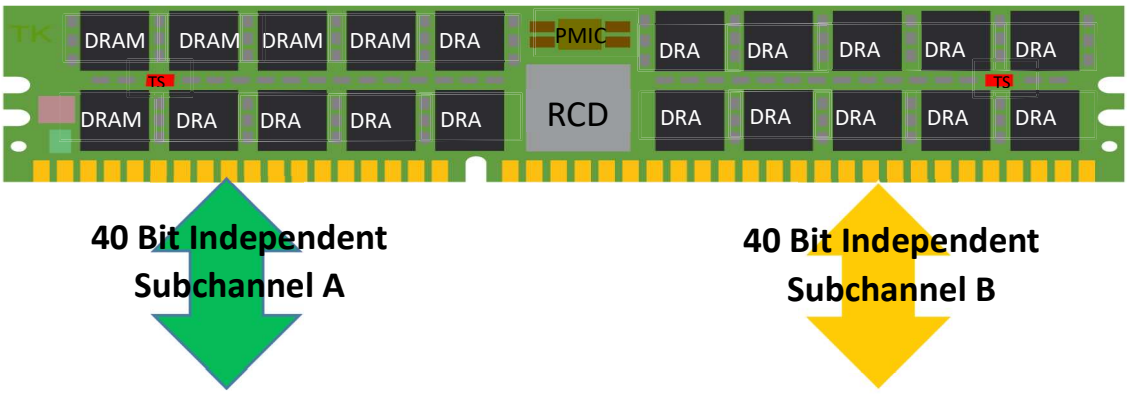


**Figure 1: DDR5 2Rx4 RDIMM module illustrating two independent subchannels**

To achieve the same data payload as a DDR4 module per transaction with the subchannel module layout, the DDR5 default burst length (BL) has increased from 8 to 16. The doubling of the BL implies a halving of data inputs/outputs (I/Os) required to fulfill the same amount of data for a given system access size. This enables the two independent subchannels on the module. The independent subchannels increase concurrency and support better scheduling from the memory controller.

As an example, each subchannel allows for 32 data I/Os with a BL of 16 resulting in 64-byte payloads. A read operation from the combined channels results in an output of 128 bytes.

## Voltage Regulation on the Module

DDR5 modules introduce local voltage regulation on the module. The voltage regulation is achieved by a power management integrated circuit (PMIC). The PMIC provides the brains of a smart voltage regulation system for the DDR5 DIMM, enabling configurability of voltage ramps and levels as well as current monitoring. Power management has been historically done on the motherboard. The introduction of PMICs allows additional features like threshold protection, error injection capabilities, programmable power on sequence, and power management features. The presence of the PMIC on the module enables better power regulation and reduces complexity of the motherboard design by reducing the scope of DRAM power delivery network (PDN) management.

## Sideband Access

DDR5 introduces sideband access to non-DRAM module bill-of-materials (BOM) active components. The sideband access is based on the MIPI I3C® sideband communication protocol with backward compatibility to I2C. Due to the growth in the number of active components on the DDR5 module, a serial presence detect (SPD) hub was introduced. The SPD hub acts as a secondary to the system host sideband and as a primary to the remaining active DIMM components. The SPD hub also contains the programmable read-only memory (PROM) pertaining to the SPD. The I3C protocol also scales up the bandwidth on the sideband bus. The SPD hub interacts with the external controller and also decouples the load of the internal bus from that of the external control bus, while providing local access to the registered clock driver (RCD), PMIC and temperature sensor integrated circuits (ICs).

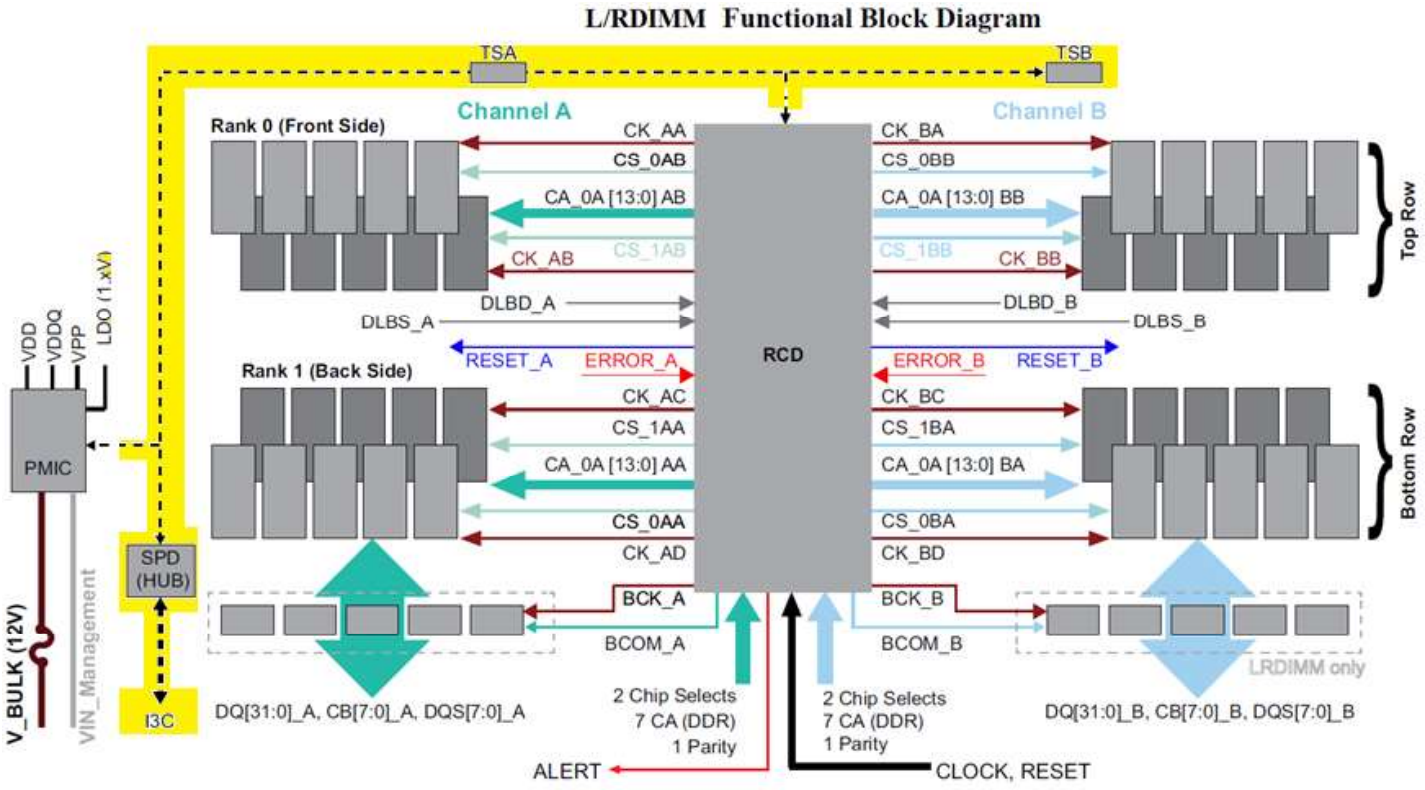


**Figure 2: Functional Block Diagram of RDIMM and LRDIMM Memory**

### Temperature Sensor IC's on DIMM

DDR5-based registered DIMMs (RDIMMs) and load-reduced DIMMs (LRDIMMs), often written together as L/RDIMMs (Figure 2), have added two integrated circuit (IC) temperature sensors, called TS1/TS2. The purpose of this feature is to give additional capability to monitor thermal changes across the length of each DIMM. Each temperature sensor is placed strategically near each end of the DIMM, embedded between the memory components (Figure 3). These new temperature sensors can be monitored via the I2C/I3C bus at a regular cadence based on host requirements. Accessing these temperature sensors via the sideband I2C/I3C bus can reduce traffic needed on the system in-band channel to monitor temperature update flags from each DRAM until a temperature threshold is approaching. Systems can also manipulate the TS1/TS2 sensors for fan speed changes to ensure data access does not need to be throttled.

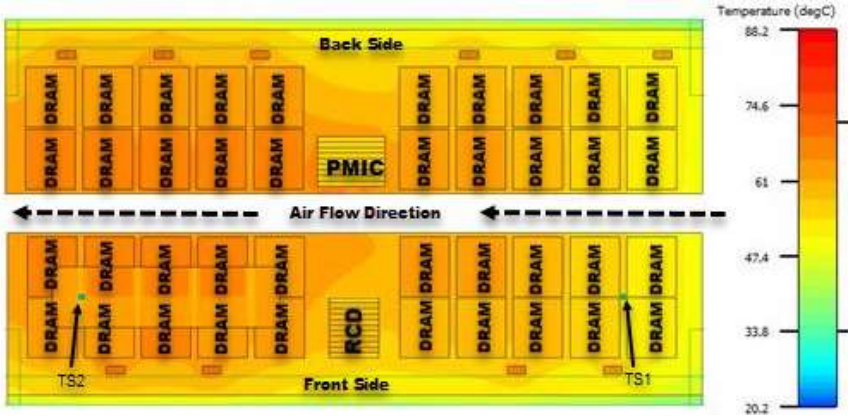


**Figure 3: Thermal Gradient Across DIMM**

# Architectural Effects on L/RDIMM Pin Definition

Several functional and architectural changes were made to DDR5 L/RDIMMs to maintain the same 288-edge pin count found on DDR4 DIMMs, while innovating to overcome challenges seen by DDR4 designs. Adding features such as command address invert (CAI) and mirror (MIR) are two examples. Including a different power delivery solution to the DIMM and adding a double data rate (DDR) command/address (CA) bus definition have freed up additional pins for isolation enhancements. These changes show up in the pin definition differences between a standard DDR4 L/RDIMM and the DDR5 L/RDIMM (Table 1).

**Table 1: Pin Differences Between DDR4 and DDR5 L/RDIMMs**

| Overview of L/RDIMM Pin Condition Changes | | | |
|---|---|---|---|
| **Pin Type** | DDR4 | DDR5 | Note |
| **VDD** | 26 – VDD | 3 – 12V (bulk) | Reduces overall power pins |
| **VSS** | 94 | 127 | Increased ground for SI; signals are all VSS referenced |
| **VTT/VPP/VREF/VDDSPD** | 9 | 0 | PMIC supports all these rails |
| **Command/Address** | 27 + CS | 2 x 7 (DDR) + CS | Seven DDR CA pins per subchannel; plus, chip select (CS) pin |
| **Data I/Os** | 72 | 80 | Support for separate subchannels |

Reducing the number of power rail and CA pins allows adding more VSS ground pins to improve DDR5 VSS-referenced signal crosstalk as well as other signal-integrity challenges caused by increasing the overall system bandwidth.

DDR5 components introduced the CAI feature, which allows the option to invert the 14-pin single data rate (SDR) CA bus states for one-cycle and two-cycle DRAM commands (Figure 4). The CAI pin on the DRAM device will be tied/strapped low (de-asserted) or high (asserted) on the board or module. For example, an RCD can drive the upper row of components CA bus noninverted and the lower row of components inverted, providing a significant reduction in power delivery noise.

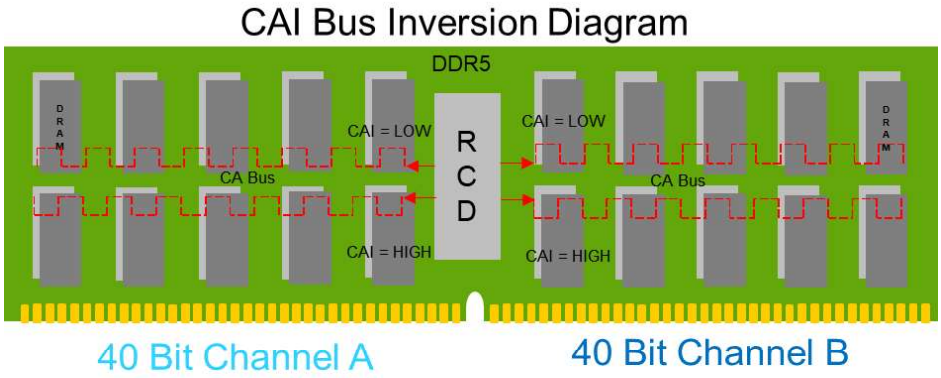


**Figure 4: Registered Clock Driver (RCD) With Command/Address Inversion Pin Feature**

DDR5 components also introduced the MIR pin. When the MIR pin is high, the DDR5 SDRAM internally swaps even-numbered CA balls with the next higher odd-numbered CA balls. This swap is symmetrical across the gap of columns in the middle of the DRAM package, as shown in Figure 5 below. This swap allows for minimal trace stubbing of the CA nets to DRAMs on opposite sides of the module for “clamshell” placements of DRAMs on the front and backside of the DIMM printed circuit board (PCB). Components on the front side of a module would have the MIR pin strapped in an opposite state from the component on the backside of the module.

MIR-pin-enabled, CA-ball-pair examples: CA2 swaps with CA3 (not CA1), CA4 swaps with CA5 (not CA3).

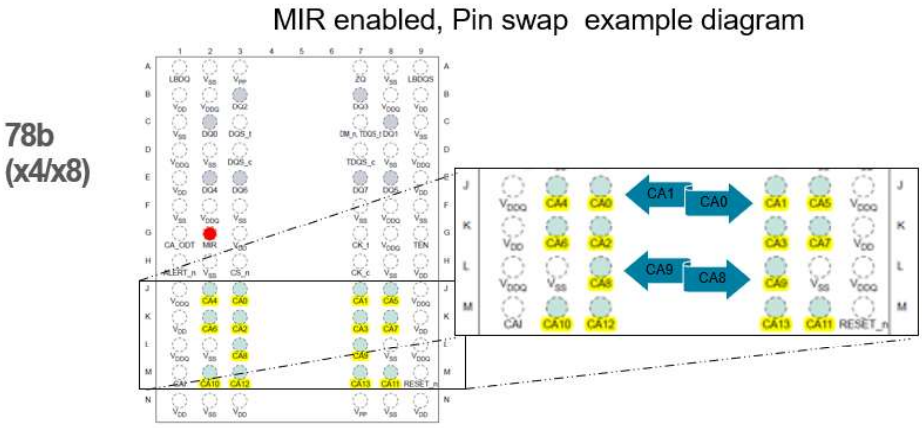


**Figure 5: Pop-out Showing Pin Swaps on a MIR-Enabled DDR5 Component**

# DDR5 On-Die Termination Improvement

DDR5 module designs incorporate the same basic routing topologies for all I/O, address, control/command, and clock signals that DDR4 did.

- The familiar input/output (DQ) and input/output strobe (DQS) pins are all direct routed from the edge connector or data buffer.
- Clock, command, and address pins are fly-by routed from the RCD.

The difference is in the termination method: discrete on DDR4 vs. on-die termination (ODT) on DDR5.

- DDR4 uses discrete termination resistors on the modules/boards for command clock (CK), chip select (CS), CA and other control pins.
- DDR5 added the benefit of programmable ODT for CK, CS, and CA, as well as a per-device configurable CA_ODT pin.

The CA_ODT pin is a new feature on each DDR5 SDRAM device allowing the last DRAM on a CS, CA, or CK net to have a comparatively strong ODT setting (40 ohms) and all the remaining DRAM on the CS, CA, or CK net to have weak or disabled (ODT) settings (Figure 6). The CA_ODT pin can be tied/strapped high or low on the board/DIMM to enable one of two different groupings, which have mode-register-programmable ODT levels. Typical DIMM or board usage applies a weak termination setting to Group A devices nearer to the controller and a stronger termination setting to Group B devices nearer the end of the fly-by routing.

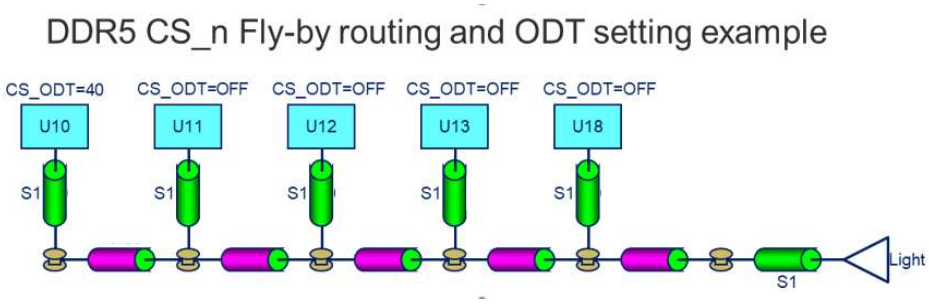


**Figure 6: Additional Routing Technologies for a DDR5**

## DDR5 CS, CA, DQ, and DQS Bus Training

Along with ODT benefits to help with fly-by routes on the DIMM/board, DDR5 also added abilities to train the CS and CA buses.

Variation in bus routing on a module/board between a signal bus and a reference signal such as the CS vs. clock pin or DQs to DQS opens innovation for solutions to train out the differences.

## Chip Select Training Mode

On entering chip select training mode (CSTM), the system drives continuous no-operation (NOP) commands on the bus. CSTM along with NOP commands on the CA bus ensures that no invalid commands are sent to DRAMs.

The CS signal sweeps while capturing multiple samples of four continuous CS states, which are clock sampled and evaluated. If the evaluated four-state sample is equivalent to “0-1-0-1,” then the CSTM sets DQ pins to a low state. All samples that are not equivalent to “0-1-0-1” cause DQs to be set to a high state. Training multiple device

CS windows without exiting CSTM helps to compromise the CK to CS timing relationship. Adjusting the CS timing window per device improves margins and stability.

### Command/Address Training Mode

Command/address training mode (CATM) enables training the CA net without risk of invalid commands being sent to the DRAM. After entering CATM, multiple iterations of the CA bus are sent, with a seed of only one pin in the bus in a high or low state. The bus is sampled and the exclusive-or (XOR) gate is evaluated. An XOR evaluation outcome that is equal to "1" sets the DQ pins to a low state; all other evaluation outcomes will be equal to "0" and the CATM will set the DQ bus to a high state. Each device on the module or board is trained to maximize CA bus pin windows. The overall benefit of this training is an increased CA signal window and improved bus stability during operation.

## DQ/DQS Training

The training of DQ and DQS is done in a multiphase set of routines using newly defined loopback pins. These individual routines, such as read training, read preamble training and write level training, align DQS pins to DQ pins and center align these to a reference clock. The DQ/DQS Tx and Rx are then trained using new multi-tap decision-feedback-equalization (DFE) settings to adjust for crosstalk and noise on the channel and improve data eye width. VrefDQ global and per-bit training are used to adjust the signal for data eye height. To combat the effects of voltage and temperature shifts on the DRAMs, a DQS interval oscillator helps signal to the system when it may need to retrain. These methods and new features are used to accommodate the stringent bit error rate (BER) eye metric required as data rates increase.

## Summary

Several architectural and protocol changes, as well as innovative new features, were instrumental in bringing about this exciting Micron DDR5 memory-based L/RDIMM module solution.

The independent subchannel architecture unlocks the data throughput needed to meet expected increased computing needs in server applications. A PMIC added on the module improves power regulation, reduces motherboard complexity, and brings a better DIMM-level power delivery. I3C-capable sideband access to all the active integrated support devices enhances usability while still monitoring the critical parameters to keep the power, thermals and system-critical details available. A pair of temperature sensor ICs strategically placed on the L/RDIMM enables constant monitoring of gradient-module-surface temperatures, easing system in-band traffic and allowing for more system-usable transactions. The DDR5 module design overhaul inspired several additional new features like CAI, MIR and expanded grounding, which significantly improved design layout, power noise and module signal isolation.

New features like ODT on commands and addresses and enhanced DQ/DQS/CA/CS training provide for better signaling performance, faster clock rates, and eventually, enhanced bandwidth. The increased memory bandwidth in DDR5 will help computing achieve new milestones.

**For more information** on Micron's DDR5 and other memory products, visit micron.com/products/dram.

# Authors


## Neal Koyle

As principle architect for Micron's compute and networking memory devices, Neal Koyle is engaged in the memory industry community, helping drive to completion the development of the first DDR5 SDRAM memory specification. Koyle pulls from a 26-year Micron Technology memory products-based career with experience on a range of products, including SRAM, SDRAM, DDR2 SDRAM, Mobile DDR2 SDRAM, and RLDRAM.

## Sujeet Ayyapureddi

As principle engineer in product architecture for Micron's compute and networking memory devices, Sujeet Ayyapureddi has been innovating with DRAM for the last 18 years. He holds a master's degree in electrical engineering.


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